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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/530,553	07/21/2000	GERALD DEBOY	POO0578	6916

7590 02/03/2003

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EXAMINER
BROCK II, PAUL E

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 02/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/530,553	DEBOY ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16 and 20-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16 and 20-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Information Disclosure Statement

1. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Drawings

2. The corrected or substitute drawings were received on December 2, 2002. These drawings are approved.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 16 and 20 – 33 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. It is not clear where in the originally filed specification

support for "said at least on e floating guard ring surrounding the high voltage region;" can be found. Further, it is not clear where in the originally filed specification support for "a low voltage portion of said substrate," can be found. And still, it is not clear where in the originally filed specification support for "at least one inner ring of a first conductivity type defining a ring structure around said ... high voltage semiconductor component(s)," can be found.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 16 – 26 and 29 – 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Hsu et al. (USPAT 5521105, Hsu).

With regard to claim 16, Hsu discloses in figure 1 a high voltage semiconductor component. Hsu discloses in figure 1 a semiconductor body having a high voltage region with the high voltage semiconductor component and having an edge region of the high voltage region, a high voltage resistant structure at the edge region having at least one inner zone (12) of a first conductivity type adjacent to a first surface of said semiconductor body. As far as the examiner can ascertain, Hsu discloses in figure 1 at least one floating guard ring (18) of a second conductivity type arranged in said inner zone, said at least one floating guard ring surrounding the high voltage region. Hsu discloses in figure 1 inter-ring zones (19) of said first conductivity type respectively arranged in said inner zone, said inter-ring zones being allocated in pairs to

each of said floating guard rings, said inter-ring zones being arranged laterally such that they separate two respective consecutive floating guard rings from one another. Hsu discloses in figure 1 wherein at least one of said floating guard rings and said inter-ring zones have at least one of conductivities and geometries set such that their free charge carriers are totally depleted when a blocking voltage is applied.

With regard to claim 20, Hsu discloses in figure 1 wherein said floating guard rings have one of a U-shaped cross section.

With regard to claim 21, Hsu discloses in figure 1 at least one space charge zone stopper located at an outermost edge of said edge region of said semiconductor component.

With regard to claim 22, Hsu discloses in figure 1 wherein said space charge zone stopper comprises a heavily doped region (16) of said first conductivity type, said heavily doped region being arranged in said inner zone.

With regard to claim 23, Hsu discloses in figure 1 wherein said space charge zone stopper comprises a damage implanted region (16) being arranged in said inner zone.

With regard to claim 24, Hsu discloses in figure 1 wherein said space charge zone stopper comprises an electrode (23) connected to said inner zone, said electrode being polysilicon.

With regard to claim 25, Hsu discloses in figure 1 at least one magnetoresistor located at an inner edge of said edge region of said semiconductor component.

With regard to claim 26, Hsu discloses in figure 1 wherein at least one of said magnetoresistors is simultaneously a gate electrode of said semiconductor component.

With regard to claim 29, Hsu discloses in figure 1 wherein said inter-ring zones in said edge region have a cross-section tapered to said first surface.

With regard to claim 30, Hsu discloses in figure 1 wherein the semiconductor component is a vertical power transistor.

With regard to claim 31, Hsu discloses in figure 1 a semiconductor chip. Hsu discloses in figure 1 at least one high voltage semiconductor component in the substrate. As far as the examiner can ascertain, Hsu discloses in figure 1 an edge structure at an edge of the high voltage semiconductor component, the edge structure separating a high voltage portion of the substrate from a low voltage portion of the substrate, the edge structure including: at least on inner-zone of a first conductivity type defining a ring structure around the at least one high voltage semiconductor component at the major surface; floating guard rings of a second conductivity type arranged in the at least on inner zone; and inter-ring zones of the first conductivity type arranged in the at least one inner zone, the inter-ring zones being allocated in pairs to each of the floating guard rings, the inter-ring zones being arranged laterally so as to separate two respective consecutive floating guard rings from one another. Hsu discloses in figure 1 at least one of the inter-ring zones and the floating guard rings being of a at least on of a conductivity and a geometry such that their free charge carriers are totally depleted when a blocking voltage is applied.

With regard to claim 32, Hsu discloses in figure 1 a semiconductor chip. Hsu discloses in figure 1 a substrate having a major surface/ Hsu discloses in figure 1 a plurality of high voltage semiconductor components in the substrate. Hsu discloses in figure 1 an edge structure at an edge of the plurality of high voltage semiconductor components to separate the high voltage semiconductor components from a remainder of the substrate, the edge structure including: at least one inner zone of a first conductivity type defining a ring structure around the plurality of

high voltage semiconductor components at the major surface; at least one floating guard ring of a second conductivity type arranged in the at least on inner zone; inter-ring zones of the first conductivity type arranged in the at least one inner zone, the inter-ring zones being allowed in pairs to each of the at least one floating guard ring, the inter-ring zones being arranged laterally so as to separate two respective consecutive floating guard rings from one another. Hsu discloses in figure 1 at least one of the inter-ring zones and the floating guard rings being of a at least on of a conductivity and a geometry such that their free charge carriers are totally depleted when a blocking voltage is applied.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu as applied to claims 16 and 25 above and further in view of Ludikhuize (USPAT 5883413).

With regard to claim 27, Hsu teaches in figure 2g that an outermost of the magnetoresistor is enclosed by a cathode metallization (60) in a direction of the first surface of the semiconductor component. Hsu does not teach that the outermost of a magnetoresistors is nearly completely enclosed by a cathode metallization. Ludikhuize teaches in figure 1 wherein at least an outermost of a magnetoresistors is nearly completely enclosed by a cathode metallization (10) in a direction of a first surface of a semiconductor component (4). It would have been

obvious to one of ordinary skill in the art at the time of the present invention to use the cathode metallization of Ludikhuize in the method of Hsu in order to reduce peaks in the localized electric field, thereby increasing the breakdown voltage of the transistor.

With regard to claim 28, Hsu teaches in figure 2g wherein said cathode metallization is a metallization of a source electrode of said semiconductor component.

Response to Arguments

9. Applicant's arguments filed December 2, 2002 have been fully considered but they are not persuasive.

10. With regard to the applicant's arguments that in Hsu "only islands or a stripe are mentioned," it should be noted that Hsu teaches other structures as well, for example, see figure 1. Therefore, the arguments are not persuasive, and the rejection is proper.

11. With regard to the applicant's arguments that there "is no suggestion or disclosure that the island structures of Hsu are at an edge region of the component," it should be noted that there is nothing in the claims or written description that distinguishes the claimed edge region over the island structures of Hsu. With a quick review of the written description, the claims, and Hsu it is clear that any indication of the "edge" of the region is clearly the same "edge" in all of these. A mere ascertation that the edge region is different than the island regions of Hsu can only be supported by direct evidence from the originally filed disclosure and claimed limitations

supporting the disclosure. No such evidence has been presented. Therefore, the arguments are not persuasive, and the rejections are proper.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
January 28, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
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